REMARKS

Claims 3-14,16-20, 22-27 and 31 are pending. Claims 21 and 32 are canceled without prejudice or disclaimer. Claims 3-5, 8-11, 13, 19 and 26 are amended. A marked-up version showing the changes to the claims made by the present amendment is attached hereto as **"Version with markings to show changes made."**

Claims 3, 4, 7-14, 16, 18-25 and 32 were rejected under 35 USC § 112, second paragraph, as being indefinite. The claims have been amended to no longer refer to a percent carbon. As such, it is believed that the amended claims are in full compliance with 35 USC § 112.

Claims 7, 8, 16, 18, 19, 22, 24 and 25 were rejected under 35 USC § 102(b) as being anticipated by ***Yu et al.*** and were rejected under 35 USC § 102(e) as being anticipated by ***Shepard***. Claims 3-5, 7-14, 16, 19-27 and 32 were rejected under 35 USC § 103(a) as being unpatentable over ***Brennan et al.*** Favorable reconsideration of these rejections is requested in view of the amendments made herein.

The claims have been amended to specify an organic SOG film as the first insulating film. None of the cited references teaches or suggests that planarization is effected by polishing after impurities such as argon ions are introduced into a surface of an organic SOG film as the first insulating film. ***Shepard***, ***Brennan et al.*** or ***Yu et al.*** discloses that planarization is effected after boron or phosphorous ions are implanted into a silicon oxide film formed using TEOS as the material by CVD.

The present invention is directed to an improvement of the process of achieving a favorable planarized surface of an appropriate level by planarization using an organic SOG film and then polishing the planarized surface by CMP for further planarization. In contrast, the

processes disclosed by ***Yu et al.***, ***Brennan et al.*** or ***Shepard*** are directed to planarization using only silicon oxide film formed with the material of TEOS by CVD method. According to the present invention, it is possible to achieve a favorable planarized surface of an appropriate level by planarization using an SOG film as well as to embed an insulating film in a microminiaturized interconnection without any gap, in comparison with using an insulating film formed by CVD method. Further, polishing rate of the SOG film is improved to a level substantially equal to the polishing rate of a silicon oxide film formed by CVD, with preventing defects from being generated in the surface of the SOG film by polishing after previously implanting impurities such as argon ions into the SOG film. Such effects as described above are would not have been expected by a person skilled in the art.

Yu et al. (Abstract and Table 1) and ***Brennan et al.*** (column 5, lines 54-58) disclose that the polishing rate of the TEOS film is improved by implanting impurities into the TEOS film. None of the cited references, however, discloses or suggests that the polishing rate of the SOG film is improved to a level substantially equal to the polishing rate of a silicon oxide film such as TEOS film formed by CVD. Thus, it would not have been obvious for a person skilled in the art to employ a SOG film in place of the TEOS film in ***Yu et al.*** , ***Shepard*** or ***Brennan et al.***

Figs. 20-22 of the present application illustrate the unexpected results associated with the claimed invention. These figures show that the moisture and the hydroxyl group included in an organic SOG film are reduced by the conversion of the organic SOG film 5 into a modified SOG 7 by ion implantation. Page 15, lines 7 through page 17, line 19 of the present specification discuss the results illustrated in Figs 20-22.

For at least the foregoing reasons, the presently claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by applicants would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone applicants' undersigned attorney.

In the event that this paper is not timely filed, applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

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Attachment: Version with markings to show changes made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE (08/921,250)

IN THE CLAIMS:

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Claims 3-5, 8-11, 13, 19 and 26 have been amended as follows:

3. (Three Times Amended) The fabrication method of a semiconductor device according to claim [32] 8, wherein said step of planarization comprises the step of effecting [planrization] planarization by polishing said first and second insulation films.

4. (Three Times Amended) The fabrication method of a semiconductor device according to claim [32] 8, wherein said second insulation film includes a silicon oxide film formed by plasma CVD.

5. (Twice Amended) A fabrication method of a semiconductor device comprising the steps of:

forming a first insulation film on a substrate,

forming a second insulation film, including at least an organic SOG film, on said first insulation film,

introducing impurities at least to a surface of said first insulation film either before or after forming said second insulation film, and

effecting planarization by polishing at least said second insulation film,

wherein said step of introducing impurities comprises the steps of

forming a photoresist on a surface of a device before impurities are introduced to said first insulation film, and

introducing impurities into said first insulation film via said photoresist film.

8. (Three Times Amended) A fabrication method of a semiconductor device comprising the steps of:

forming a first insulation film on a substrate,

forming a second insulation film, including at least an organic SOG film, on said first insulation film,

introducing impurities at least to a surface of said first insulation film either before or after forming said second insulation film, and

effecting planarization by polishing at least said second insulation film[,

wherein said first insulation film includes a silicon dioxide material containing at least 1% of carbon].

9. (Three Times Amended) The fabrication method of a semiconductor device according to claim [32] 8, wherein said first insulation film includes a material having a contact angle of purified water of not more than 30° with respect to said first insulation film.

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10. (Three Times Amended) The fabrication method of a semiconductor device according to claim [32] 8, wherein said first insulation film includes an inorganic SOG film.

11. (Three Times Amended) The fabrication method of a semiconductor device according to claim [32] 8, wherein said polishing is carried out by chemical mechanical polishing.

13. (Three Times Amended) The fabrication method of a semiconductor device according to claim [32] 8, wherein said step of introducing impurities comprises the step of introducing impurities into said first insulation film by implantation.

19. (Twice Amended) A fabrication method of a semiconductor device comprising the steps of:

forming a first insulation film, including at least an organic SOG film, on a substrate,

introducing impurities at least to a surface of said first insulation film, and

effecting planarization by polishing said first insulation film[,

wherein said first insulation film includes a silicon oxide material containing at least 1% of carbon].

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26. (Three Times Amended) A fabrication method of a semiconductor device comprising the steps of:

forming a first insulation film, including at least an organic SOG film, on a substrate,

forming a second insulation film on said first insulation film,

effecting planarization by polishing at least said second insulation film by chemical mechanical polishing using an abrasive liquid including a surfactant , and

introducing impurities into said first insulation after said polishing step.